



# PASTRY

Phase Change Memory Advanced universal Switches through Thin alternating laYers

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## Objective

The project aims at exploiting the potential of engineered Chalcogenide Super Lattices (CSL) to achieve a breakthrough in power dissipation and switching speed of Phase Change Memories, toward the realization of a "universal memory".

## Consortium



### Lower Power Consumption

- Lower consumption
- Lower Voltage required by CMOS
- More relaxed requirements on diode



### Better Reliability

- Higher endurance thanks to lower thermal stress
- Higher reliability of interconnect
- Lower potential disturbs

July 2012: PCM enters volume production regime



Universal Memory key attributes	Flash NAND	DRAM	Conventional PCM	STT MRAM	RRAM
4F2 cell size	A	N	P	N	A
Fast write/erase	N	A	P	A	A
Non volatility	A	N	A	A	A
Extended endurance	N	A	P	A	P
Fast access time	N	A	A	A	A
Bit granularity	P	A	A	A	A
Power consumption	A	N	P	P	A
Readiness for production	A	A	A	P	N
Scalability	P	P	A	A	A

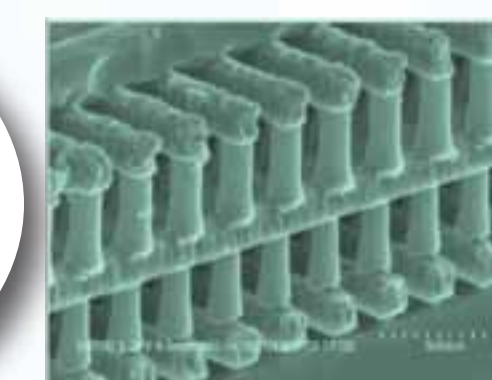
### Better Array Efficiency

- Smaller HV circuitry (pump, decoders)
- Lower parasitic voltage drop (larger tiles)

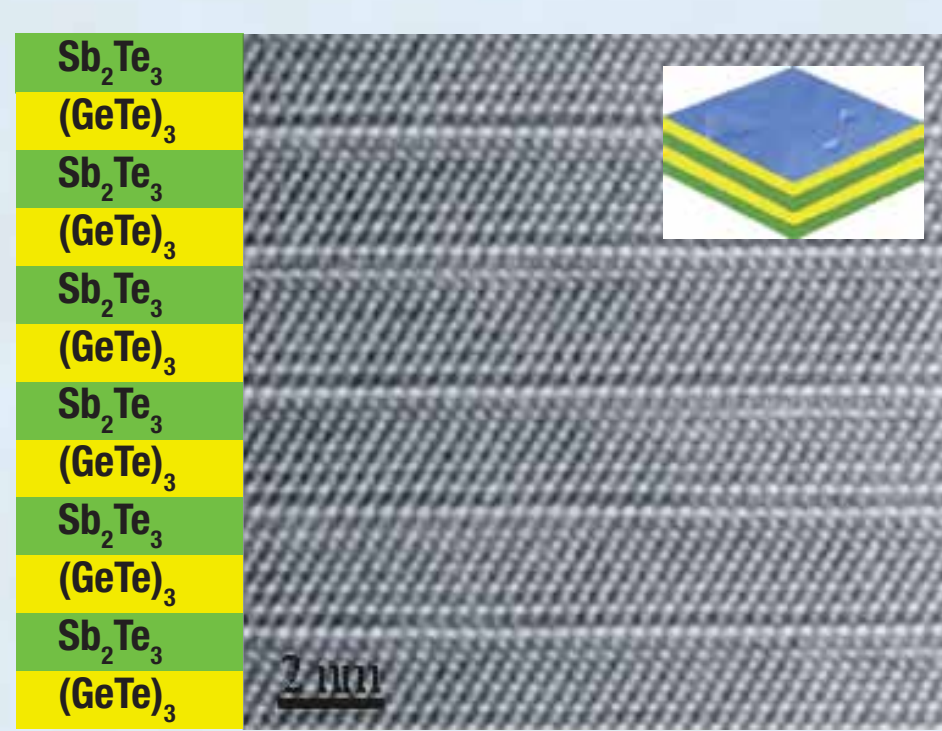


### Multilayer capability

- Low current density diodes enabled
- Stacking of more than one memory layers



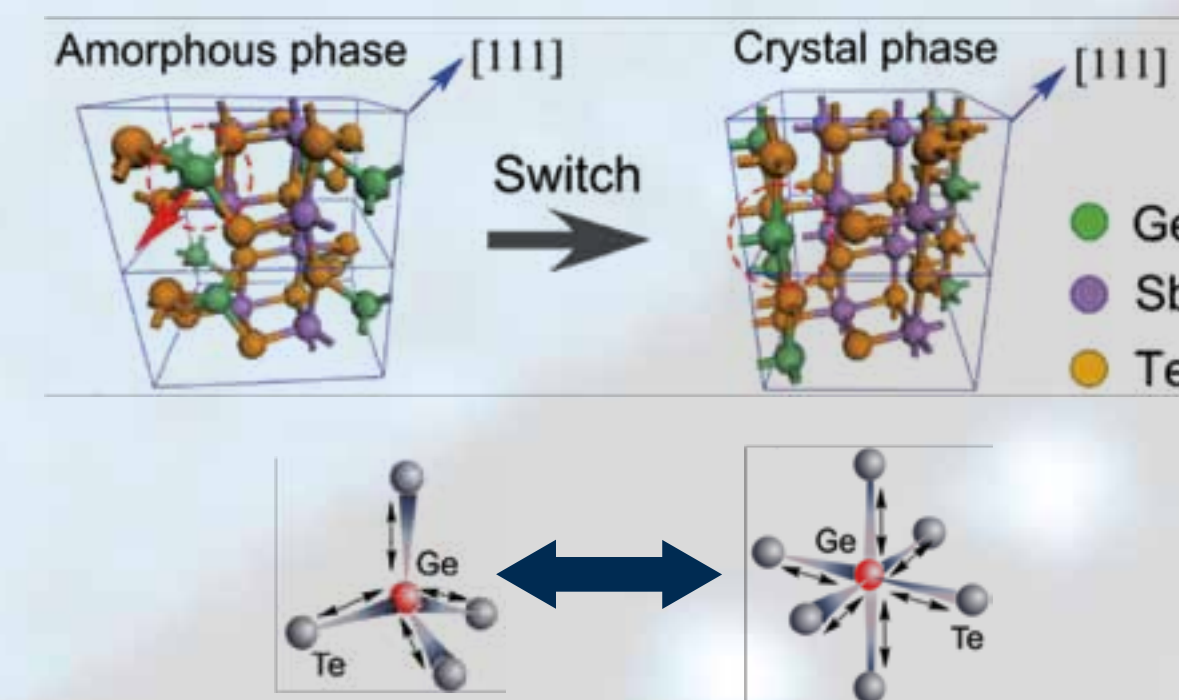
The programming current reduction in Phase-Change Memory (PCM) represents a performance enabler and allows several breakthrough areas...



HRTEM image: Ge<sub>3</sub>Sb<sub>2</sub>Te<sub>6</sub> as an alternation of 3 GeTe double layers and 1 Sb<sub>2</sub>Te<sub>3</sub> stacking sequence

**Chalcogenide Super-Lattice (CSL)** concept is based on a transition between the low and the high conductive states of the memory via a **change in the local atomic bonding**, likely enabled by confinement effects, preventing the pure mass melting. Temperature seems not to be required to increase above the melting point of the alloy, thus **enabling a reduction of the programming current and the optimization of low power memory concepts**.

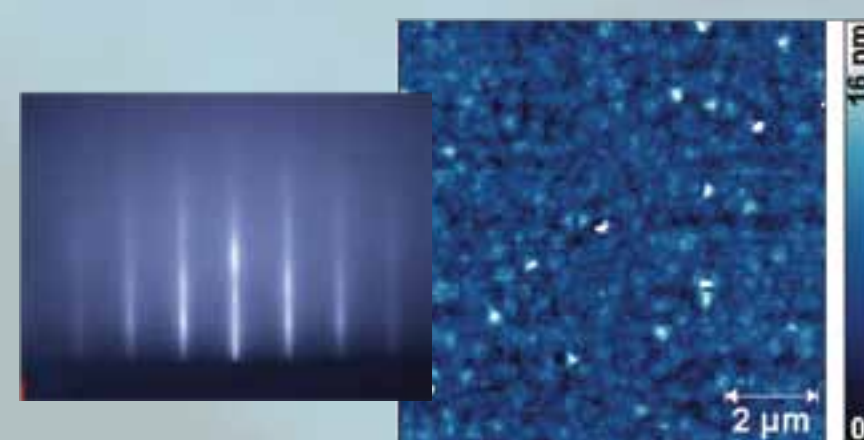
Example of a switching mechanism based on the field-driven position shift of a Ge atom



## Work Packages Description

### WP2

Material development



- **Superlattice deposition development:** Molecular Beam Epitaxy (MBE) and Physical Vapor Deposition (PVD) techniques will be used.
- **Physical characterization of materials:** Advanced characterization techniques such as X-Ray Diffraction, Secondary Ion Mass Spectrometry, Auger Electron Spectroscopy, High Resolution TEM will be used to study the realized films.
- **Optimization of CSL deposition:** progress is expected by CSL layer thickness and roughness reduction, interface electrical and thermal resistance optimization.

### WP3

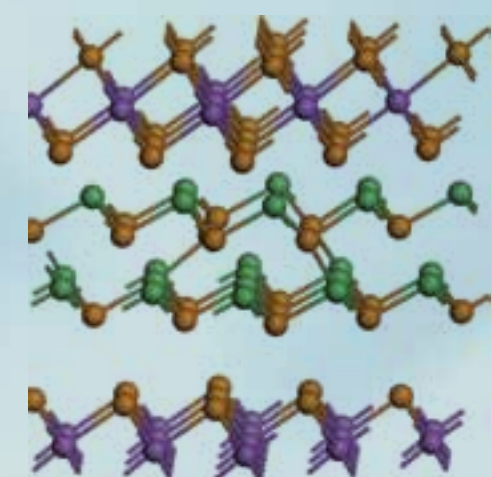
Device development



- **Development of cell test vehicle:** memory cells with different stack compositions will be developed to test the CSLs.
- **Electrical characterization and reliability:** electrical characterization tests including IV, programming curves and reliability will be performed on the developed CSLs.
- **Characterization of optimized stack:** an optimized stack will be identified starting from a benchmark of the electrical device parameters and results from WP2. Such optimized stack will be extensively characterized.

### WP4

Physical charact. and modelling



- **Development of CSL model:** a description of the system at the atomic level will be done. Modelling of the transport properties of the conductive and insulating states via simulations will be provided.
- **Physical characterization of CSL states:** HRTEM will be used to assess the CSL physical structure; EXAFS, transient XAS and Raman spectroscopy to understand the local atomic environment.
- **Modelling of the switching mechanism:** during the project the switching mechanism will be experimentally studied and a model will be provided with the help of simulation tools.

### WP5

Demonstrator



- **Modelling of device and array:** a model for the CSL device will be elaborated starting from WP4 understanding. Array simulations will be done, enabling the design of CSL array demonstrator.
- **Memory array demonstrator:** final goal of the project is the fabrication of a large-scaled (1-4 Gbit) demonstrator at the state of the art 2x node, never reported so far for CSL.
- **Scaling potential:** Scaling rules of programming current, power and energy, switching times, retention and endurance will be provided, allowing scaling projections for next generation chip fabrication.



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